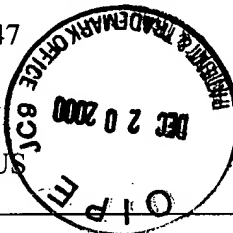


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#14
1203-01
DRS

Applicant(s): Mark I. Gardner, Robert Dawson, H. Jim Fulford, Jr., Frederick N. Hause, Mark
W. Michael, Bradley T. Moore, Derick J. Wristers
Assignee: Advanced Micro Devices, Inc.
Title: Dopant Diffusion-Retarding Barrier Region Formed Within Polysilicon Gate
Layer
Serial No.: 09/177,047 Filing Date: October 22, 1998
Examiner: A. Ghyka Group Art Unit: 2812
Docket No.: M-4692 US Client Ref. No.: TT1618

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San Jose, California
December 20, 2000

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Washington, D. C. 20231

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR § 1.97(b)

Dear Sir:

Pursuant to 37 C.F.R. § 1.56, § 1.97 and § 1.98, the documents listed on the accompanying PTO Form-1449 are called to the attention of the Examiner for the above patent application. Copies of these documents are enclosed.

Citation of these documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

EXPRESS MAIL LABEL NO:

EL708268675US

Respectfully submitted,

David G. Dolezal
Attorney for Applicant(s)
Reg. No. 41,711

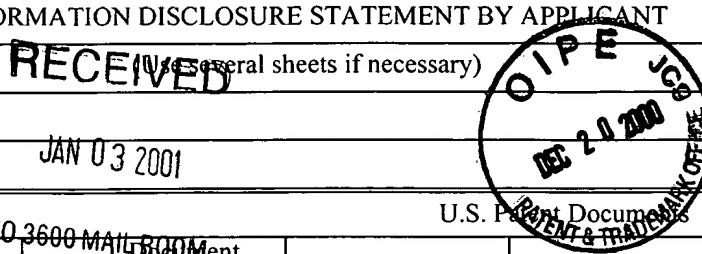
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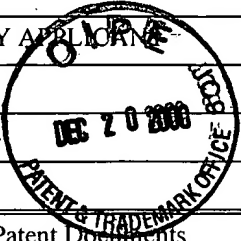
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U.S. Department of Commerce, Patent and Trademark Office					Atty Docket No.		Serial No.	
					M-4692 US		09/177,043	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applicant(s)			
RECEIVED (Use several sheets if necessary) JAN 03 2001					Mark I. Gardner, et al.			
					Filing Date		Group	
					October 22, 1998		2812	
TO 3600 MAIL ROOM U.S. Patent & Trademark Office								
*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate		
	AA	4,369,072	Jan. 18, 1983	Bakeman, Jr. et al.	148	1.5		
	AB	4,420,872	Dec. 20, 1983	Solo de Zaldivar	29	571		
	AC	4,481,527	Nov. 6, 1984	Chen et al.	357	23		
	AD	4,575,921	March 18, 1986	Bhagat	29	571		
	AE	4,623,912	Nov. 18, 1986	Chang et al.	357	54		
	AE	4,774,197	Sep. 27, 1988	Haddad et al.	437	27		
	AG	4,869,781	Sep. 26, 1989	Euen et al.	156	643		
	AH	4,897,368	Jan. 30, 1990	Kobushi et al.	437	200		
	AI	5,219,773	June 15, 1993	Dunn	437	42		
	AI	5,324,960	June 28, 1994	Pfiester et al.	257	67		
	AK	5,436,481	July 25, 1995	Egawa et al.	257	324		
Foreign Patent Documents								
							Translation	
	Document	Date	Country	Class	Subclass	Yes	No	
	AL							
	AM							
	AN							
	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ	H. Fang, et al., "Low Temperature Furnace-Grown Reoxidized Nitrided Oxide Gate Dielectrics as a Barrier to Boron Penetration," IEEE Electron Device Letters, vol. 13, no. 4, Apr. 1992, pp. 217-219						
	AR	A. B. Joshi, J. Ahn and D. L. Kwong; "Oxynitride Gate Dielectrics for p+-Polysilicon Gate MOS Devices," IEEE Electron Devices Letters, vol. 14, no. 12, December 1993, pages 560-562.						
	AS	Chuan Lin et al., "Leakage Current, Reliability Characteristics, and Boron Penetration of Ultra-Thin (32-36Å) O ₂ Oxides and N ₂ O/NO Oxynitrides," International Electron Devices Meeting Technical Digest, December 8-11, 1996, San Francisco, CA, pages 331-334.						
Examiner			Date Considered					
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.								

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TO 3600 MAIL ROOM U.S. Patent Documents								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
	AA	5,518,958	May 21, 1996	Giewont et al.	437	186		
	AB	5,605,848	Feb. 25, 1997	Ngaoaram	437	24		
	AC	5,668,028	Sep. 16, 1997	Bryant	438	287		
	AD	5,744,845	April 28, 1998	Sayama et al.	257	371		
	AF	5,872,376	Feb. 16, 1999	Gardner et al.	257	336		
	AF	5,945,719	Aug. 31, 1999	Tsuda	257	413		
	AG	5,962,904	Oct. 5, 1999	Hu	257	412		
	AH	5,977,561	Nov. 2, 1999	Wu	257	67		
	AJ	5,998,271	Dec. 7, 1999	Schwalke	438	301		
	AJ	6,040,207	March 21, 2000	Gardner et al.	438	216		
	AK							
Foreign Patent Documents								
							Translation	
		Document	Date	Country	Class	Subclass	Yes	No
	AL							
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	AO							
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ	E. Hasegawa et al., "The Impact of Nitrogen Profile Engineering On Ultra-Thin Nitrided Oxide Films for Dual-Gate CMOS ULSI," <i>International Electron Devices Meeting Technical Digest</i> , December 10-13, 1995, Washington, DC, pages 327-330.						
	AR	S.V. Hattangady, H. Niimi, and G. Lucovsky, "Controlled Nitrogen Incorporation at the Gate Oxide Surface," <i>Applied Physics Letters</i> , Vol. 66, No. 25, June 19, 1995, pages 3495-3497.						
	AS	Stanley Wolf and Richard N. Tauber, <i>Silicon Processing for the VLSI Era, Volume 1: Process Technology</i> , Lattice Press, Sunset Beach, California, 1986, pages 182-195, 209-211, 280-283, 294, 308, 321-327.						
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OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AQ	Stanley Wolf, <i>Silicon Processing for the VLSI Era, Volume 2: Process Integration</i> , Lattice Press, Sunset Beach, California, 1990, pages 124-131.					
	AR	Stanley Wolf, <i>Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET</i> , Lattice Press, Sunset Beach, California, 1995, pages 305-313, 496-504, 641-642 and 648-661.					
	AS	Hattangady, et al., "Ultrathin Nitrogen-Profile Engineered Gate Dielectric Films," <i>International Electron Devices Meeting Technical Digest 1996</i> , December 8-11, 1996, San Francisco, California, pp. 495-498.					
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<p>*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.</p>							

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	AO							
	AP							
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
	AQ	C.T. Liu et al, "High Performance 0.2µm CMOS with 25 Å Gate Oxide Grown on Nitrogen Implanted Si Substrates," <i>International Electron Devices Meeting Technical Digest</i> , San Francisco, California, December 8-11, 1996, pages 499-502.						
	AR	C.T. Liu et al, "25 Å Gate Oxide without Boron Penetration for 0.25 and 0.3-µm PMOSFETs," <i>1996 Symposium on VLSI Technology Digest of Technical Papers</i> , pages 18-19.						
	AS							
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